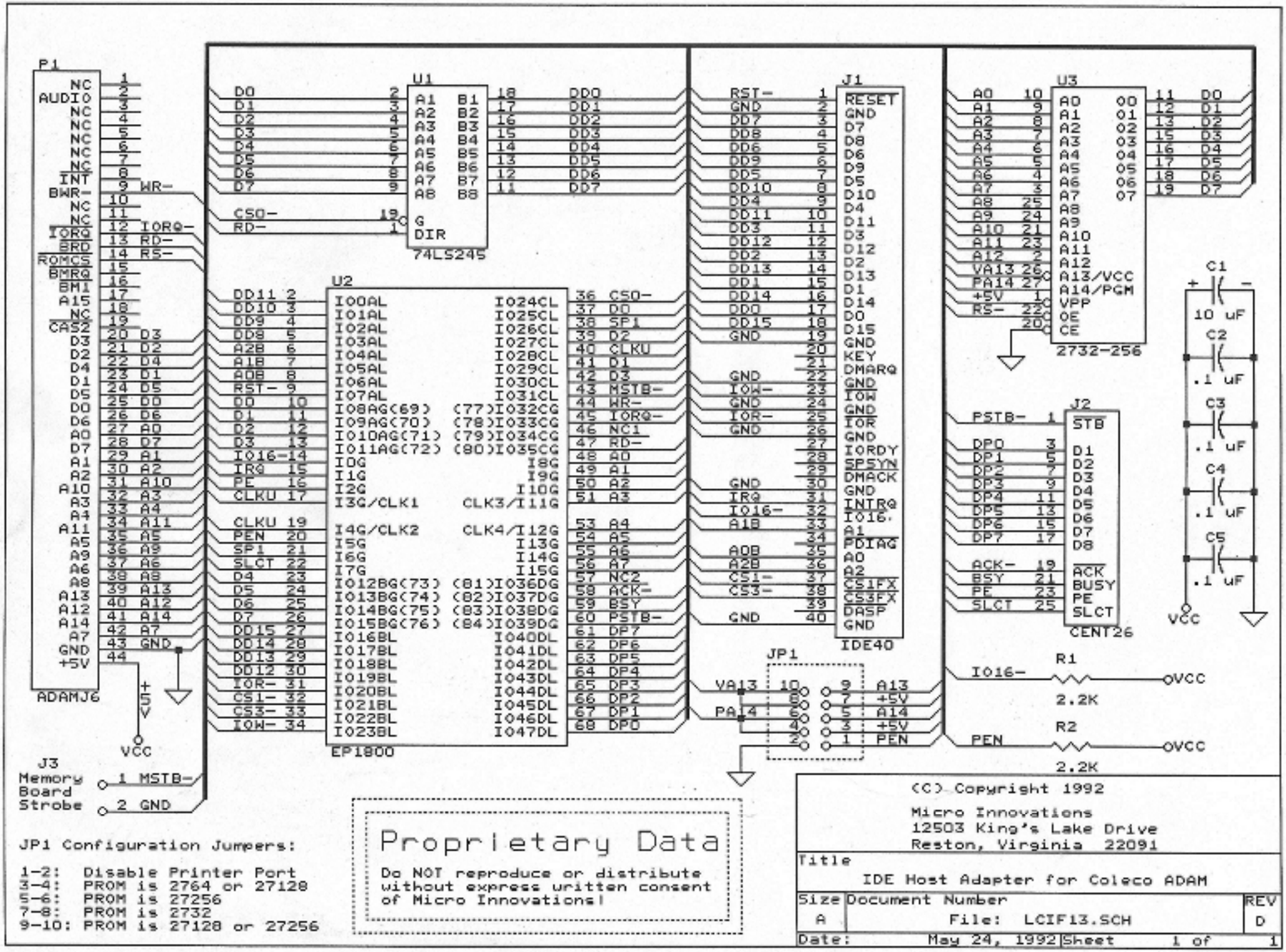
P1
ADAMJ6
U1
74LS245
U2
EP1800
J1
IDE40
U3
2732-256
J2
CENT26
JP1
C1
10 uF
C2
.1 uF
C3
.1 uF
C4
.1 uF
C5
.1 uF
R1
2.2K
R2
2.2K
VCC
+5V
J3
Memory Board Strobe
1 MSTB-
2 GND
JP1 Configuration Jumpers:
1-2: Disable Printer Port
3-4: PROM is 2764 or 27128
5-6: PROM is 27256
7-8: PROM is 2732
9-10: PROM is 27128 or 27256
Proprietary Data
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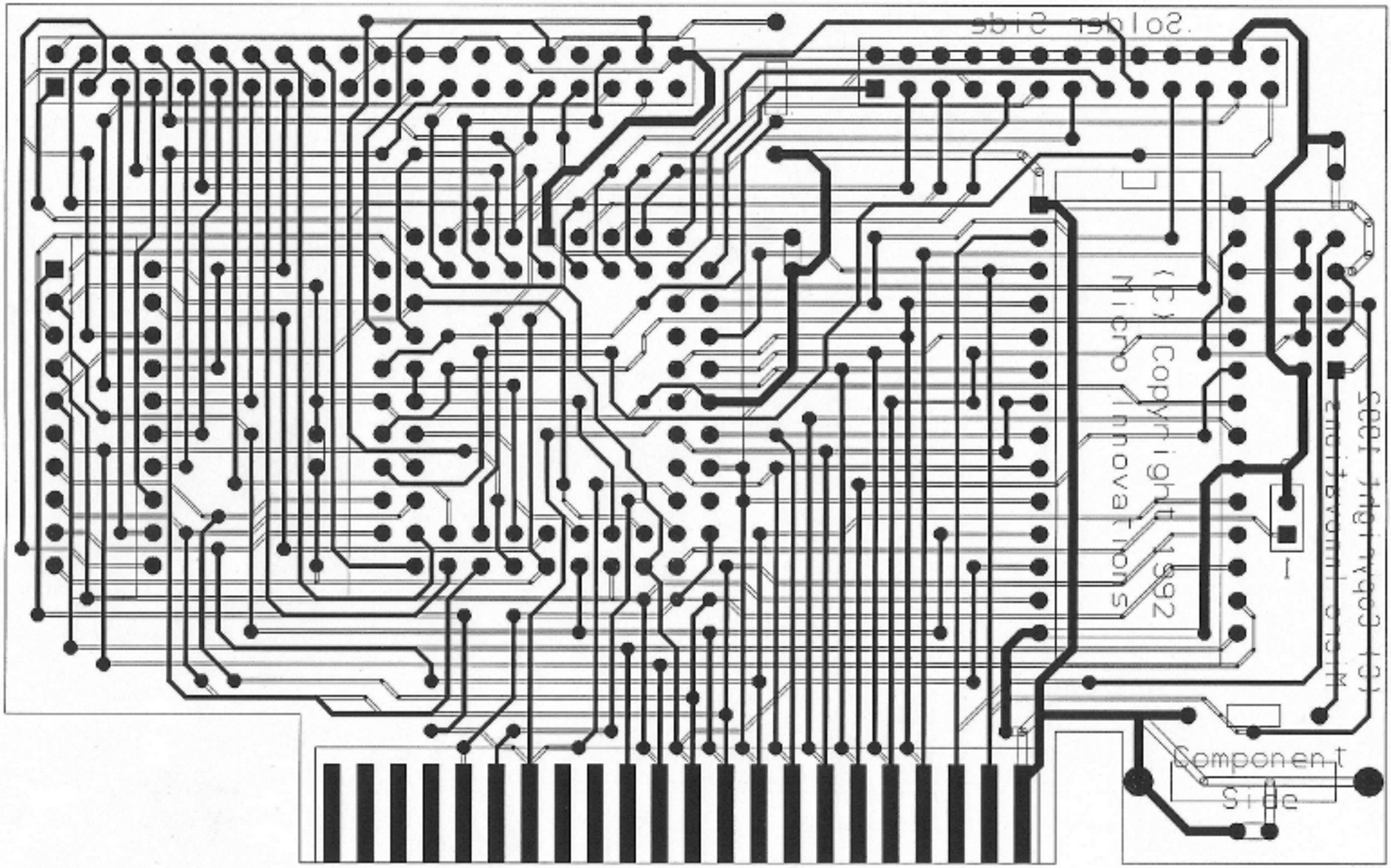
Micro Innovations
12503 King's Lake Drive
Reston, Virginia 22091
Title
IDE Host Adapter for Coleco ADAM
Size A
Document Number
File: LCIF13.SCH
REV D
Date: May 24, 1992
Sheet 1 of 1


Solder Side
(c) Copyright 1992
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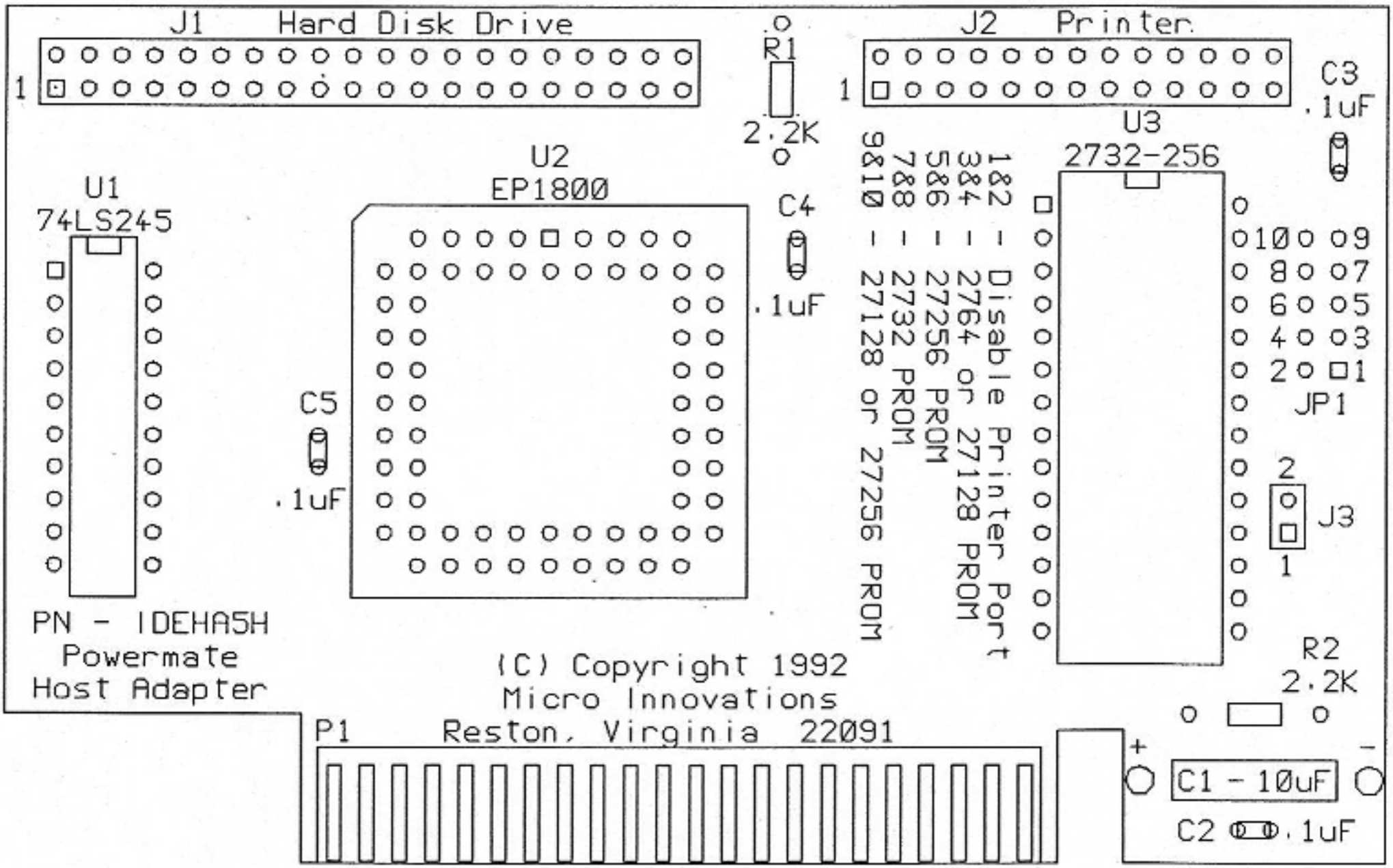
Component
Side


J1 Hard Disk Drive
1
R1
2.2K
J2 Printer
1
C3
.1uF
U3
2732-256
U2
EP1800
U1
74LS245
C4
.1uF
C5
.1uF
1&2 - Disable Printer Port
3&4 - 2764 or 27128 PROM
5&6 - 27256 PROM
7&8 - 2732 PROM
9&10 - 27128 or 27256 PROM
10 09
8 07
6 05
4 03
2 1
JP1
2
J3
1
PN - IDEHA5H
Powermate
Host Adapter
(C) Copyright 1992
Micro Innovations
Reston, Virginia 22091
R2
2.2K
P1
+
-
C1 - 10uF
C2 .1uF

```
OrCAD PLD COMPILER 386  V1.10  9/11/92  (Source file G:\ORCAD\IDE\G1810_58.PLD)

  1  File:       G1810_58.PLD
  2  Date:       August 2, 1992
  3
  4  This file contains the logic necessary for an EP1810 PLD to perform
  5  address decoding and 8/16 bit data multiplexing and demultiplexing to
  6  interface an IDE hard disk drive to the Coleco Adam computer.  The
  7  GAL also contains logic to drive a parallel printer port.
  8
  9  |EP1810c
 10   2:DD11, 3:DD10, 4:DD9, 5:DD8,    6:A2B,  7:A1B,  8:A0B,
 11   9:RST,  10:D0, 11:D1,    12:D2, 13:D3, 16:PE,
 12   17:CLK1, 19:CLK2, 20:PEN, 22:SLCT, 23:D4, 24:D5, 25:D6,
 13   26:D7, 27:DD15, 28:DD14, 29:DD13, 30:DD12, 31:IOR, 32:CS1,
 14   33:CS3, 34:IOW, 36:CS0, 37:BBSY, 39:BSLCT,
 15   40:CLKU, 41:BACK, 42:BPE, 43:MSTB, 44:WR,
 16   45:IORQ, 47:RD, 48:A0, 49:A1, 50:A2, 51:A3, 53:A4, 54:A5,
 17   55:A6, 56:A7, 58:ACK, 59:BSY, 60:PSTB, 61:DP7,
 18   62:DP6, 63:DP5, 64:DP4, 65:DP3, 66:DP2, 67:DP1, 68:DP0
 19
 20   Low: IOW, IOR, IORQ, WR, RD, CS0, CS1, CS3, MSTB, PSTB,
 21        ACK, RST, CLKU
 22
 23   Configuration:  "Pin feedback", D[0..7], DD[8..15]
 24   Configuration:  "Turbo:1"
 25
 26  Addr       Input                          Output
 27
 28  01 Error Register                  Not Used (WPC Register)
 29  02 Sector Count Register           Sector Count Register
 30  03 Sector Number Register          Sector Number Register
 31  04 Cylinder Low Register           Cylinder Low Register
 32  05 Cylinder High Register          Cylinder High Register
 33  06 SDH Register                    SDH Register
 34  07 Status Register                 Command Register
 35  58 Lower Byte Data Register        Lower Byte Data Register
 36  59 Upper Byte Data Register        Upper Byte Data Register
 37  5A Alternate Status Register       Fixed Disk Control Register
 38  5B Digital Input Register          Not Used
 39
 40  To send 16 bit data:
 41    First send upper byte to port 59H and latch it into D8-D15 FFs
 42      with CLKU, but do not enable LS245 or D8-D15 FF outputs and
 43      do not send IOW
 44    Then send lower byte to port 58H, enable LS245 and D8-D15 FF
 45      outputs, and send IOW
 46
 47  To receive 16 bit data:
 48    First read lower byte from port 58H by sending IOR and enabling
 49      LS245 outputs (latch the upper byte into D0-D7 FFs with CLKU)
 50    Then read the upper byte from port 59H by enabling D0-D7 FFs;
 51      do not enable LS245 and do not send IOR
 52
 53  |
 54   Conditioning:    (RD & IORQ & A[7..0]==59H) ?? D[0..7]
 55   Conditioning:    (WR & IORQ & A[7..0]==58H) ?? DD[8..15]
```

```
56  |
57
58  | RST      = RD & IORQ & A[7..0]==1CH   |Issue for read from 1CH
59
60    Issue IOW for write to 02-07H, 58H, and 5AH
61  | IOW      = (WR & IORQ & A[7..0]>=02H & A[7..0]<=07H)
62  |       # (WR & IORQ & A[7..0]==58H)
63  |  # (WR & IORQ & A[7..0]==5AH)
64
65    Issue IOR for read from 01-07H, 58H, 5AH, and 5BH
66  | IOR      = (RD & IORQ & A[7..0]>=01H & A[7..0]<=07H)
67  |       # (RD & IORQ & A[7..0]==58H)
68  |  # (RD & IORQ & A[7..0]==5AH)
69  |  # (RD & IORQ & A[7..0]==5BH)
70
71  | CLKU     = (WR & IORQ & A[7..0]==59H) |Issue for write to 59H or
72  |       # (RD & IORQ & A[7..0]==58H) |  read from 58H
73
74    Enable LS245 output for 01H-07H, 58H, 5AH, & 5BH (RD only)
75  | CS0      = (IORQ & A[7..0]>=01H & A[7..0]<=07H)
76  |       # (IORQ & A[7..0]==58H)
77  |  # (IORQ & A[7..0]==5AH)
78  |  # (RD & IORQ & A[7..0]==5BH)
79
80  | CS1      = (A[7..0]>=01H & A[7..0]<=07H)  |Address range 01H-07H & 58H
81  |  # (A[7..0]==58H)
82
83  | CS3      = A[7..0]==5AH # A[7..0]==5BH    |Addresses 5AH & 5BH
84
85  | A0B      = A0                                    |Buffered A0
86  | A1B      = A1                                    |Buffered A1
87  | A2B      = A2 # (A[7..0]==5AH) # (A[7..0]==5BH)  |Buffered A2
88
89  | PSTB     = PEN & WR & IORQ & A[7..0]==40H    |Printer Strobe (40H)
90  | MSTB     = WR & IORQ & A[7..0]==42H          |Memory Strobe (42H)
91
92  | D[0..3]     = dff(DD[8..11],CLK1)    |D8-11 -> D0-3 FFs on CLKU
93  | D[4..7]     = dff(DD[12..15],CLK2)   |D12-15 -> D4-7 FFs on CLKU
94  | DD[8..11]   = dff(D[0..3],CLK1)      |D0-3 -> DD8-11 FFs on CLKU
95  | DD[12..15]  = dff(D[4..7],CLK2)      |D4-7 -> DD12-15 FFs on CLKU
96  | DP[0..7]    = dff(D[0..7],PSTB')     |D0-7 -> DP0-7 FFs on PSTB'
97
98  | BBSY     = (RD & IORQ & A[7..0]==40H) ?? BSY'     |Status bit 0
99  | BACK     = (RD & IORQ & A[7..0]==40H) ?? ACK      |Status bit 1
100 | BSLCT    = (RD & IORQ & A[7..0]==40H) ?? SLCT     |Status bit 2
101 | BPE      = (RD & IORQ & A[7..0]==40H) ?? PE       |Status bit 3
102 |
103 | Signature: "G1810_58"
```

RESOLVED EXPRESSIONS (Reduction 2)

Signal name	Row	Terms
RST	70	IORQ RD A0' A1' A2 A3 A4 A5' A6' A7'
IOW	230	WR IORQ A0' A2' A3 A4 A5' A6 A7'
	231	WR IORQ A1 A3' A4' A5' A6' A7'
	232	WR IORQ A2 A3' A4' A5' A6' A7'
IOR	200	IORQ RD A0' A2' A3 A4 A5' A6 A7'
	201	IORQ RD A1 A2' A3 A4 A5' A6 A7'
	202	IORQ RD A0 A3' A4' A5' A6' A7'
	203	IORQ RD A1 A3' A4' A5' A6' A7'
	204	IORQ RD A2 A3' A4' A5' A6' A7'
CLKU	280	WR IORQ A0 A1' A2' A3 A4 A5' A6 A7'
	281	IORQ RD A0' A1' A2' A3 A4 A5' A6 A7'
CS0	240	IORQ RD A1 A2' A3 A4 A5' A6 A7'
	241	IORQ A0' A2' A3 A4 A5' A6 A7'
	242	IORQ A0 A3' A4' A5' A6' A7'
	243	IORQ A1 A3' A4' A5' A6' A7'
	244	IORQ A2 A3' A4' A5' A6' A7'
CS1	210	A0' A1' A2' A3 A4 A5' A6 A7'
	211	A0 A3' A4' A5' A6' A7'
	212	A1 A3' A4' A5' A6' A7'
	213	A2 A3' A4' A5' A6' A7'
CS3	220	A1 A2' A3 A4 A5' A6 A7'
A0B	60	A0
A1B	50	A1
A2B	40	A1 A3 A4 A5' A6 A7'
	41	A2
PSTB	390	PEN WR IORQ A0' A1' A2' A3' A4' A5' A6 A7'
MSTB	310	WR IORQ A0' A1 A2' A3' A4' A5' A6 A7'
D0	89	IORQ RD A0 A1' A2' A3 A4 A5' A6 A7'
	80	DD8
D1	99	IORQ RD A0 A1' A2' A3 A4 A5' A6 A7'
	90	DD9
D2	109	IORQ RD A0 A1' A2' A3 A4 A5' A6 A7'
	100	DD10
D3	119	IORQ RD A0 A1' A2' A3 A4 A5' A6 A7'
	110	DD11
D4	129	IORQ RD A0 A1' A2' A3 A4 A5' A6 A7'
	120	DD12

```
D5          139   IORQ  RD  A0  A1' A2' A3  A4  A5' A6  A7'
            130   DD13

D6          149   IORQ  RD  A0  A1' A2' A3  A4  A5' A6  A7'
            140   DD14

D7          159   IORQ  RD  A0  A1' A2' A3  A4  A5' A6  A7'
            150   DD15

DD8          39   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
             30   D0

DD9          29   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
             20   D1

DD10         19   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
             10   D2

DD11          9   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
              0   D3

DD12        199   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
            190   D4

DD13        189   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
            180   D5

DD14        179   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
            170   D6

DD15        169   WR  IORQ  A0' A1' A2' A3  A4  A5' A6  A7'
            160   D7

DP0         479   PSTB'
            470   D0

DP1         469   PSTB'
            460   D1

DP2         459   PSTB'
            450   D2

DP3         449   PSTB'
            440   D3

DP4         439   PSTB'
            430   D4

DP5         429   PSTB'
            420   D5

DP6         419   PSTB'
            410   D6

DP7         409   PSTB'
            400   D7
```

```
BBSY        259   IORQ  RD  A0' A1' A2' A3' A4' A5' A6  A7'
            250   BSY'

BACK        299   IORQ  RD  A0' A1' A2' A3' A4' A5' A6  A7'
            290   ACK

BSLCT       279   IORQ  RD  A0' A1' A2' A3' A4' A5' A6  A7'
            270   SLCT

BPE         309   IORQ  RD  A0' A1' A2' A3' A4' A5' A6  A7'
            300   PE
```

SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows			Activity	
			Beg	Avail	Used		
2.	DD11	23	0	10	2	High	(Registered)
3.	DD10	21	10	10	2	High	(Registered)
4.	DD9	19	20	10	2	High	(Registered)
5.	DD8	17	30	10	2	High	(Registered)
6.	A2B	15	40	10	2	High	(Three-state)
7.	A1B	13	50	10	1	High	(Three-state)
8.	A0B	11	60	10	1	High	(Three-state)
9.	RST	8	70	10	1	Low	(Three-state)
10.	D0	47	80	10	2	High	(Registered)
11.	D1	45	90	10	2	High	(Registered)
12.	D2	43	100	10	2	High	(Registered)
13.	D3	41	110	10	2	High	(Registered)
14.	-	73	-	-	-		
15.	-	71	-	-	-		
16.	PE	69	-	-	-	High	
17.	CLK1	85	-	-	-	High	(Clock)
19.	CLK2	83	-	-	-	High	(Clock)
20.	PEN	63	-	-	-	High	
21.	-	65	-	-	-		
22.	SLCT	67	-	-	-	High	
23.	D4	33	120	10	2	High	(Registered)
24.	D5	35	130	10	2	High	(Registered)
25.	D6	37	140	10	2	High	(Registered)
26.	D7	39	150	10	2	High	(Registered)
27.	DD15	9	160	10	2	High	(Registered)
28.	DD14	11	170	10	2	High	(Registered)
29.	DD13	13	180	10	2	High	(Registered)
30.	DD12	15	190	10	2	High	(Registered)
31.	IOR	16	200	10	5	Low	(Three-state)
32.	CS1	18	210	10	4	Low	(Three-state)
33.	CS3	20	220	10	1	Low	(Three-state)
34.	IOW	22	230	10	3	Low	(Three-state)
36.	CS0	22	240	10	5	Low	(Three-state)
37.	BBSY	21	250	10	2	High	(Three-state)
38.	-	19	260	10	0		(Three-state)
39.	BSLCT	17	270	10	2	High	(Three-state)
40.	CLKU	14	280	10	2	Low	(Three-state)
41.	BACK	13	290	10	2	High	(Three-state)
42.	BPE	11	300	10	2	High	(Three-state)
43.	MSTB	8	310	10	1	Low	(Three-state)
44.	WR	30	320	10	0	Low	(Three-state)
45.	IORQ	28	330	10	0	Low	(Three-state)
46.	-	27	340	10	0		(Three-state)
47.	RD	24	350	10	0	Low	(Three-state)
48.	A0	61	-	-	-	High	
49.	A1	59	-	-	-	High	
50.	A2	57	-	-	-	High	
51.	A3	81	-	-	-	High	(Clock)
53.	A4	87	-	-	-	High	(Clock)
54.	A5	75	-	-	-	High	
55.	A6	77	-	-	-	High	
56.	A7	79	-	-	-	High	

57.	-	49	360	10	0		(Three-state)
58.	ACK	50	370	10	0	Low	(Three-state)
59.	BSY	53	380	10	0	High	(Three-state)
60.	PSTB	54	390	10	1	Low	(Three-state)
61.	DP7	9	400	10	2	High	(Registered)
62.	DP6	11	410	10	2	High	(Registered)
63.	DP5	13	420	10	2	High	(Registered)
64.	DP4	15	430	10	2	High	(Registered)
65.	DP3	17	440	10	2	High	(Registered)
66.	DP2	19	450	10	2	High	(Registered)
67.	DP1	21	460	10	2	High	(Registered)
68.	DP0	23	470	10	2	High	(Registered)
69.	-	7	80	10	0		(Three-state)
70.	-	5	90	10	0		(Three-state)
71.	-	3	100	10	0		(Three-state)
72.	-	1	110	10	0		(Three-state)
73.	-	1	120	10	0		(Three-state)
74.	-	3	130	10	0		(Three-state)
75.	-	5	140	10	0		(Three-state)
76.	-	7	150	10	0		(Three-state)
77.	-	7	320	10	0		(Three-state)
78.	-	5	330	10	0		(Three-state)
79.	-	3	340	10	0		(Three-state)
80.	-	1	350	10	0		(Three-state)
81.	-	1	360	10	0		(Three-state)
82.	-	3	370	10	0		(Three-state)
83.	-	5	380	10	0		(Three-state)
84.	-	7	390	10	0		(Three-state)
				640	83	(13%)	

I200 No fatal errors found in source code.
I201 No warnings.